

- Low  $r_{DS(on)}$  . . . 5  $\Omega$
- Avalanche Energy . . . 30 mJ
- Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current
- 500-mA Typical Current-Limiting Capability
- Output Clamp Voltage . . . 50 V
- Enhanced Cascading for Multiple Stages
- All Registers Cleared With Single Input
- Low Power Consumption

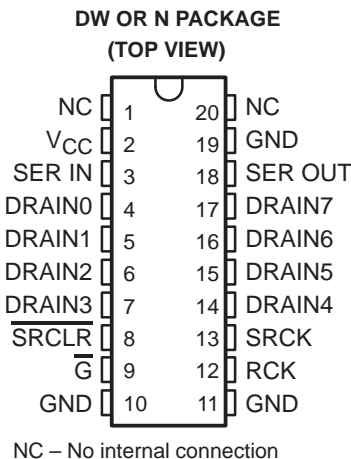
**description**

The TPIC6B596 is a monolithic, high-voltage, medium-current power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

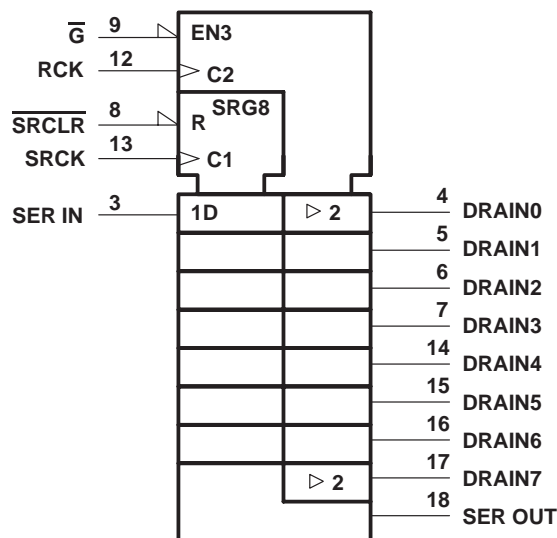
This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK), respectively. The storage register transfers data to the output buffer when shift-register clear (SRCLR) is high. When  $\overline{SRCLR}$  is low, all registers in the device are cleared. When output enable ( $\overline{G}$ ) is held high, all data in the output buffers is held low and all drain outputs are off. When  $\overline{G}$  is held low, data from the storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS-transistor outputs are off. When data is high, the DMOS-transistor outputs have sink-current capability. The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This will provide improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at  $T_C = 25^\circ\text{C}$ . The current limit decreases as the junction temperature increases for additional device protection.

The TPIC6B596 is characterized for operation over the operating case temperature range of  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .



**logic symbol†**



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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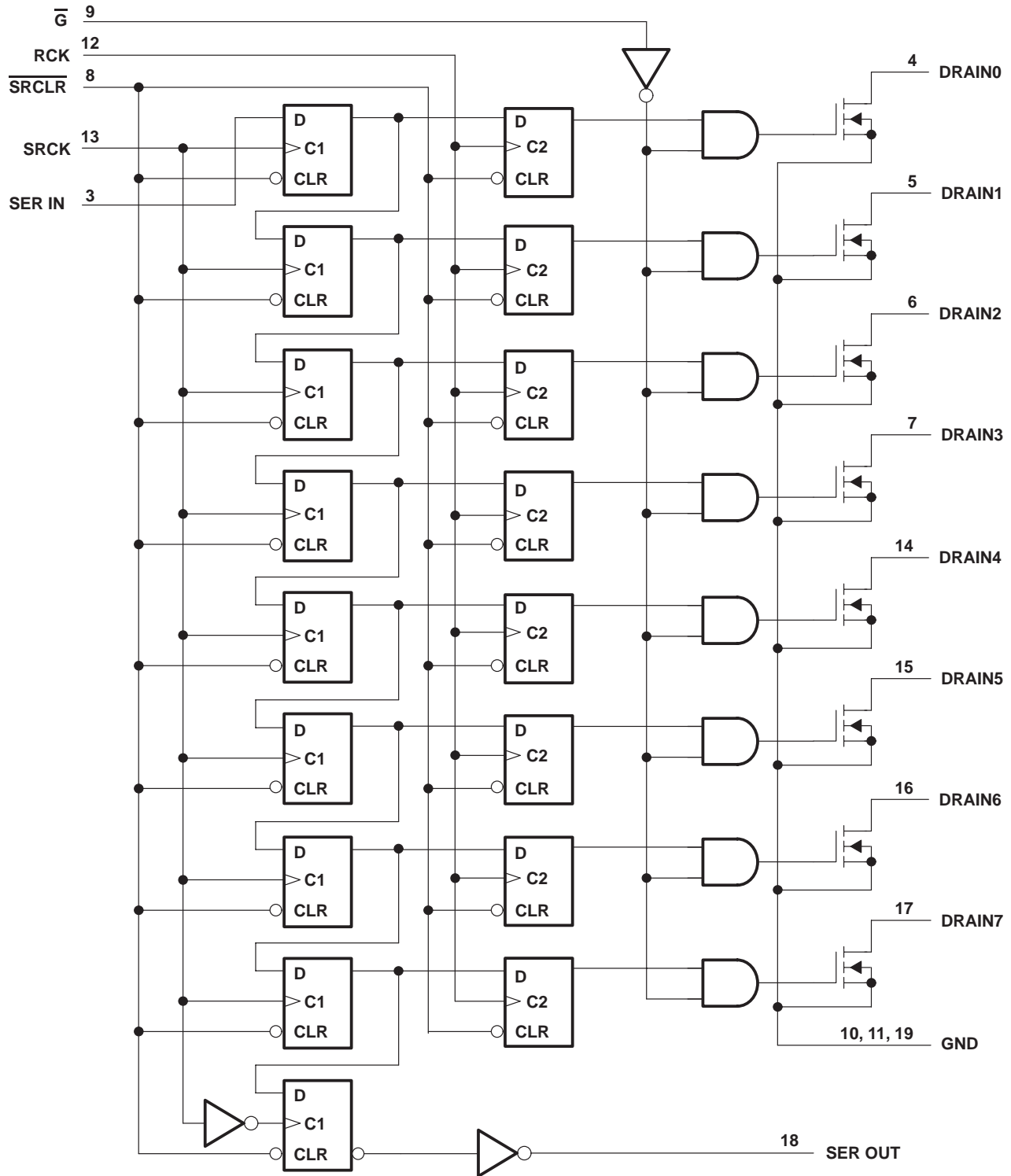
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



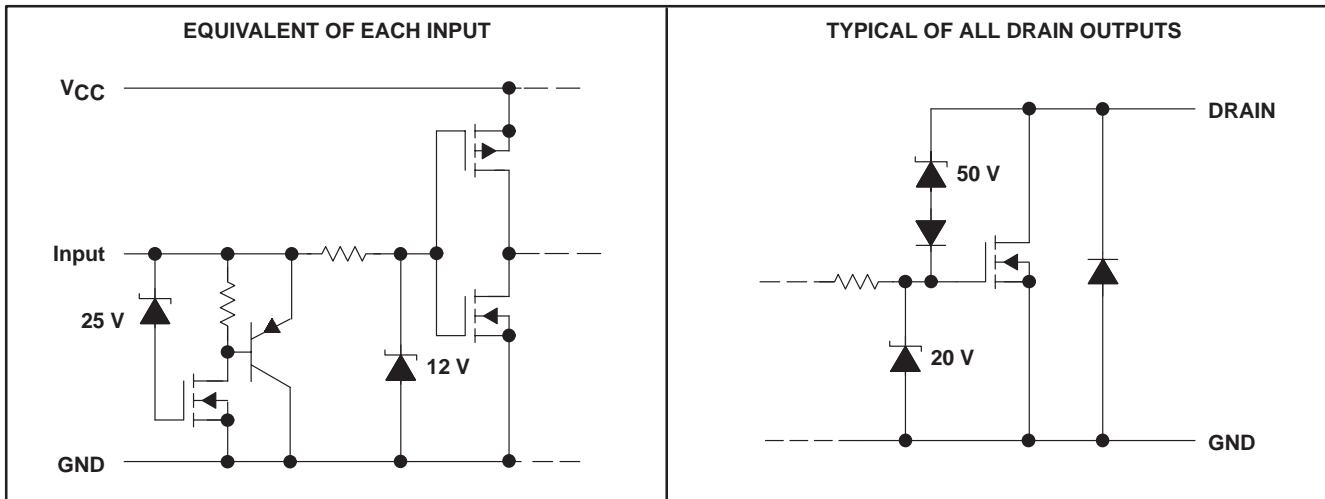
# TPIC6B596 POWER LOGIC 8-BIT SHIFT REGISTER

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## logic diagram (positive logic)



schematic of inputs and outputs



absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage, $V_{CC}$ (see Note 1)	7 V
Logic input voltage range, $V_I$	-0.3 V to 7 V
Power DMOS drain-to-source voltage, $V_{DS}$ (see Note 2)	50 V
Continuous source-to-drain diode anode current	500 mA
Pulsed source-to-drain diode anode current (see Note 3)	1 A
Pulsed drain current, each output, all outputs on, $I_D, T_C = 25^\circ\text{C}$ (see Note 3)	500 mA
Continuous drain current, each output, all outputs on, $I_D, T_C = 25^\circ\text{C}$	150 mA
Peak drain current single output, $I_{DM}, T_C = 25^\circ\text{C}$ (see Note 3)	500 mA
Single-pulse avalanche energy, $E_{AS}$ (see Figure 4)	30 mJ
Avalanche current, $I_{AS}$ (see Note 4)	500 mA
Continuous total dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, $T_J$	-40°C to 150°C
Operating case temperature range, $T_C$	-40°C to 125°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltage values are with respect to GND.
  - Each power DMOS source is internally connected to GND.
  - Pulse duration  $\leq 100 \mu\text{s}$  and duty cycle  $\leq 2\%$ .
  - DRAIN supply voltage = 15 V, starting junction temperature ( $T_{JS}$ ) = 25°C,  $L = 200 \text{ mH}$ ,  $I_{AS} = 0.5 \text{ A}$  (see Figure 4).

DISSIPATION RATING TABLE

PACKAGE	$T_C \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$	$T_C = 125^\circ\text{C}$ POWER RATING
DW	1389 mW	11.1 mW/°C	278 mW
N	1050 mW	10.5 mW/°C	263 mW

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## POWER LOGIC 8-BIT SHIFT REGISTER

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### recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, $V_{CC}$	4.5	5.5	V
High-level input voltage, $V_{IH}$	0.85 $V_{CC}$		V
Low-level input voltage, $V_{IL}$	0.15 $V_{CC}$		V
Pulsed drain output current, $T_C = 25^\circ\text{C}$ , $V_{CC} = 5\text{ V}$ (see Notes 3 and 5)	-500	500	mA
Setup time, SER IN high before SRCK $\uparrow$ , $t_{SU}$ (see Figure 2)	15		ns
Hold time, SER IN high after SRCK $\uparrow$ , $t_H$ (see Figure 2)	15		ns
Pulse duration, $t_W$ (see Figure 2)	40		ns
Operating case temperature, $T_C$	-40	125	$^\circ\text{C}$

NOTES: 3. Pulse duration  $\leq 100\ \mu\text{s}$  and duty cycle  $\leq 2\%$ .  
 5. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.

### electrical characteristics, $V_{CC} = 5\text{ V}$ , $T_C = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$ Drain-to-source breakdown voltage	$I_D = 1\text{ mA}$	50			V
$V_{SD}$ Source-to-drain diode forward voltage	$I_F = 100\text{ mA}$		0.85	1	V
$V_{OH}$ High-level output voltage, SER OUT	$I_{OH} = -20\ \mu\text{A}$ , $V_{CC} = 4.5\text{ V}$	4.4	4.49		V
	$I_{OH} = -4\text{ mA}$ , $V_{CC} = 4.5\text{ V}$	4	4.2		
$V_{OL}$ Low-level output voltage, SER OUT	$I_{OL} = 20\ \mu\text{A}$ , $V_{CC} = 4.5\text{ V}$		0.005	0.1	V
	$I_{OL} = 4\text{ mA}$ , $V_{CC} = 4.5\text{ V}$		0.3	0.5	
$I_{IH}$ High-level input current	$V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}$			1	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_{CC} = 5.5\text{ V}$ , $V_I = 0$			-1	$\mu\text{A}$
$I_{CC}$ Logic supply current	$V_{CC} = 5.5\text{ V}$	All outputs off	20	100	$\mu\text{A}$
		All outputs on	150	300	
$I_{CC}(\text{FRQ})$ Logic supply current at frequency	$f_{SRCK} = 5\text{ MHz}$ , $C_L = 30\text{ pF}$ , All outputs off, See Figures 2 and 6		0.4	5	mA
$I_N$ Nominal current	$V_{DS(\text{on})} = 0.5\text{ V}$ , $I_N = I_D$ , $T_C = 85^\circ\text{C}$		90		mA
$I_{DSX}$ Off-state drain current	$V_{DS} = 40\text{ V}$ , $V_{CC} = 5.5\text{ V}$		0.1	5	$\mu\text{A}$
	$V_{DS} = 40\text{ V}$ , $V_{CC} = 5.5\text{ V}$ , $T_C = 125^\circ\text{C}$		0.15	8	
$r_{DS(\text{on})}$ Static drain-source on-state resistance	$I_D = 100\text{ mA}$ , $V_{CC} = 4.5\text{ V}$		4.2	5.7	$\Omega$
	$I_D = 100\text{ mA}$ , $T_C = 125^\circ\text{C}$ , $V_{CC} = 4.5\text{ V}$		6.8	9.5	
	$I_D = 350\text{ mA}$ , $V_{CC} = 4.5\text{ V}$		5.5	8	

NOTES: 5. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.  
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.  
 7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at  $T_C = 85^\circ\text{C}$ .



switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_C = 25^\circ\text{C}$

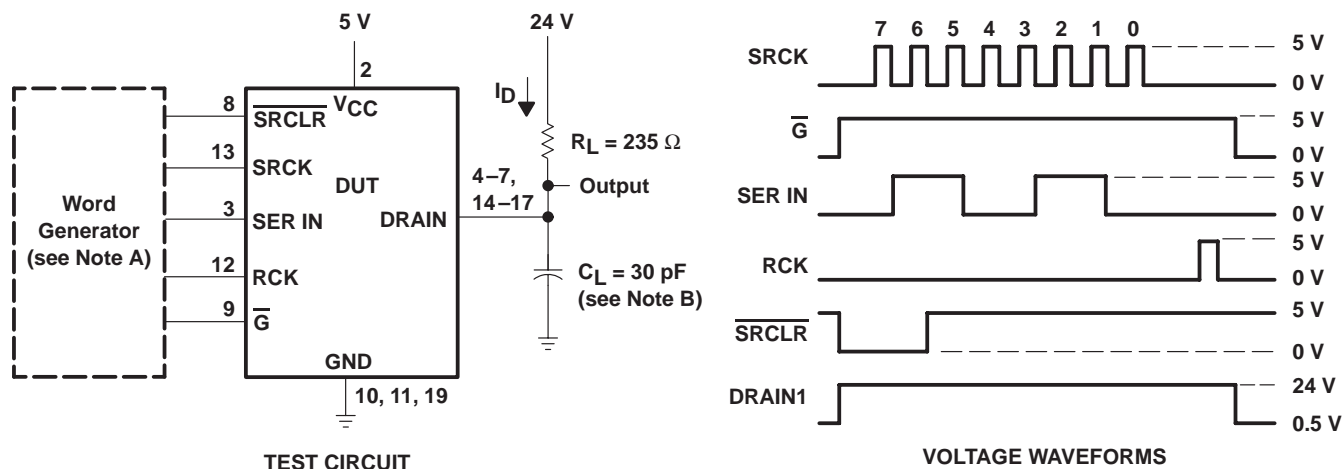
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output from $\overline{G}$	$C_L = 30\text{ pF}$ , $I_D = 100\text{ mA}$ , See Figures 1, 2, and 9		150		ns
$t_{PHL}$	Propagation delay time, high-to-low-level output from $\overline{G}$			90		ns
$t_r$	Rise time, drain output			200		ns
$t_f$	Fall time, drain output			200		ns
$t_{pd}$	Propagation delay time, SRCK $\downarrow$ to SEROUT	$C_L = 30\text{ pF}$ , See Figure 2		15		ns
$f(\text{SRCK})$	Serial clock frequency	$C_L = 30\text{ pF}$ , See Note 8			10	MHz
$t_a$	Reverse-recovery-current rise time	$I_F = 100\text{ mA}$ , $di/dt = 20\text{ A}/\mu\text{s}$ , See Notes 5 and 6 and Figure 3		100		ns
$t_{rr}$	Reverse-recovery time			300		

- NOTES: 5. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.  
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.  
 8. This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows for SRCK  $\rightarrow$  SEROUT propagation delay and setup time plus some timing margin.

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW package		90	$^\circ\text{C}/\text{W}$
		N package		95	

PARAMETER MEASUREMENT INFORMATION



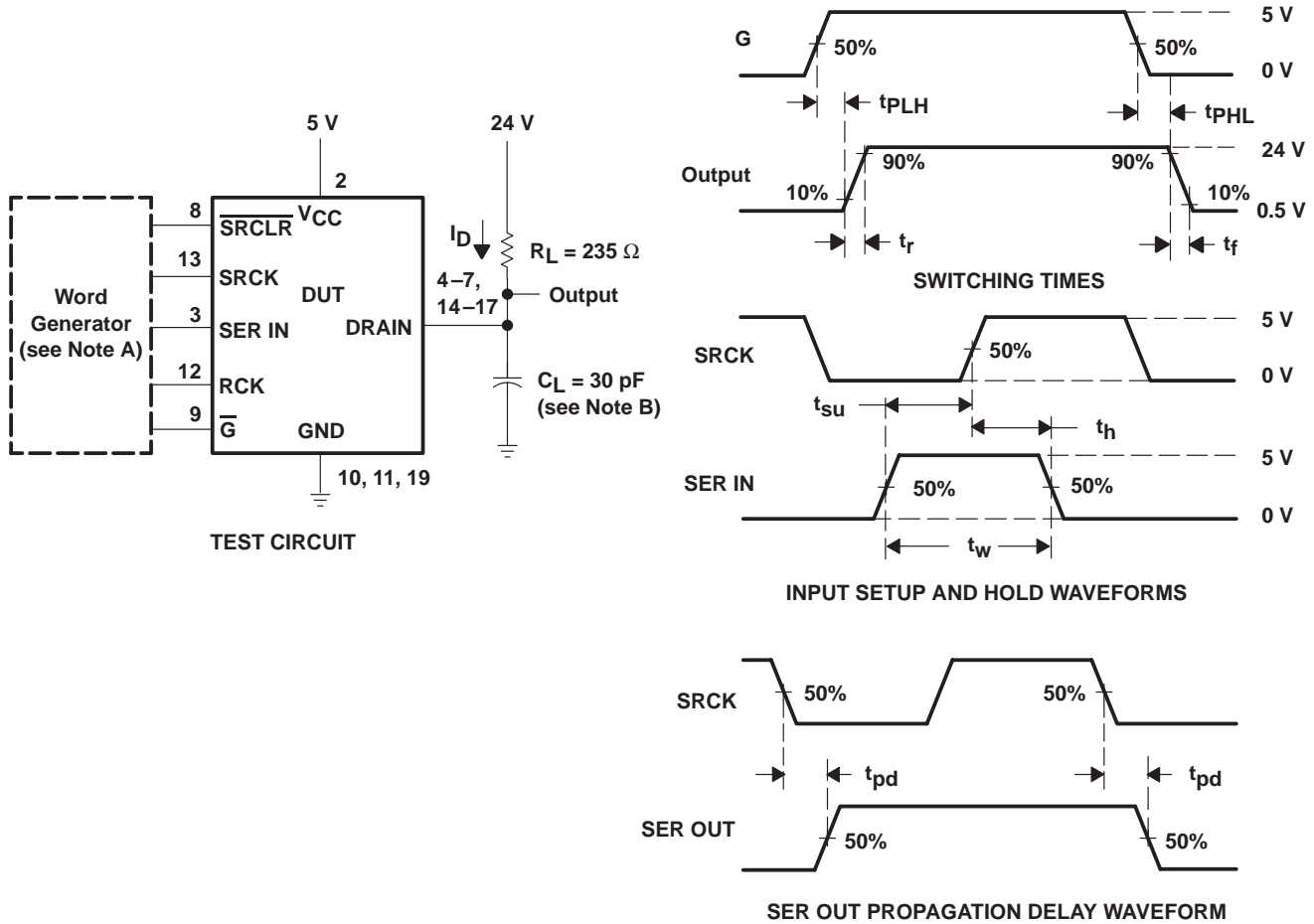
- NOTES: A. The word generator has the following characteristics:  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ ,  $t_w = 300\text{ ns}$ , pulsed repetition rate (PRR) = 5 kHz,  $Z_O = 50\ \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

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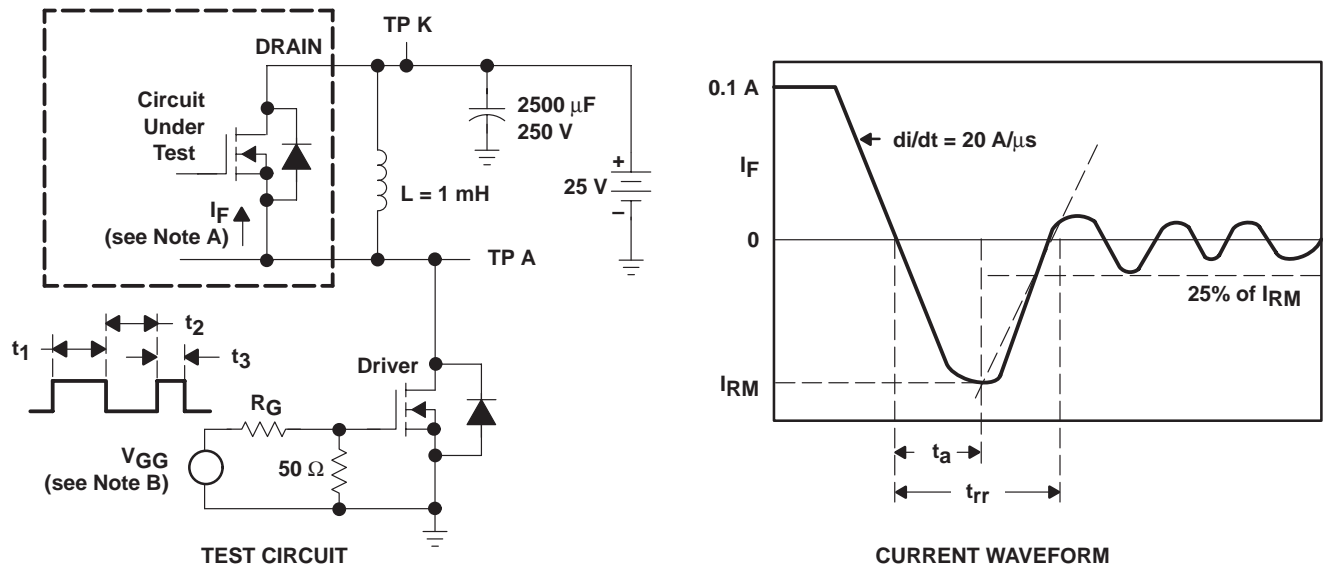
## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The word generator has the following characteristics:  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ ,  $t_w = 300 \text{ ns}$ , pulsed repetition rate (PRR) = 5 kHz,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

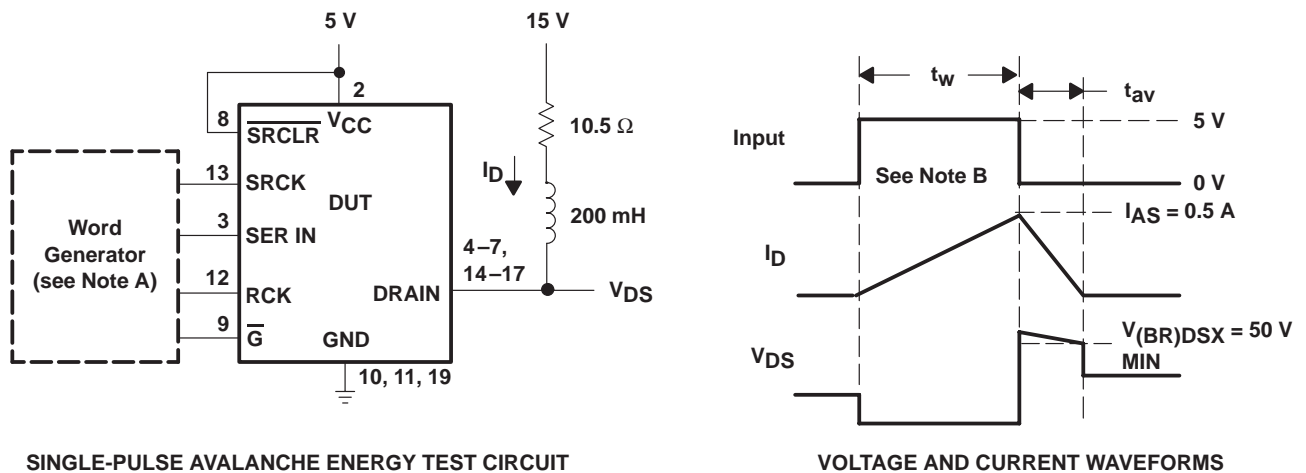
**Figure 2. Test Circuit, Switching Times, and Voltage Waveforms**

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.  
 B. The  $V_{GG}$  amplitude and  $R_G$  are adjusted for  $di/dt = 20 \text{ A}/\mu\text{s}$ . A  $V_{GG}$  double-pulse train is used to set  $I_F = 0.1 \text{ A}$ , where  $t_1 = 10 \mu\text{s}$ ,  $t_2 = 7 \mu\text{s}$ , and  $t_3 = 3 \mu\text{s}$ .

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode



- NOTES: A. The word generator has the following characteristics:  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ ,  $Z_O = 50 \Omega$ .  
 B. Input pulse duration,  $t_w$ , is increased until peak current  $I_{AS} = 0.5 \text{ A}$ .  
 Energy test level is defined as  $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30 \text{ mJ}$ .

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

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## TYPICAL CHARACTERISTICS

PEAK AVALANCHE CURRENT  
vs  
TIME DURATION OF AVALANCHE

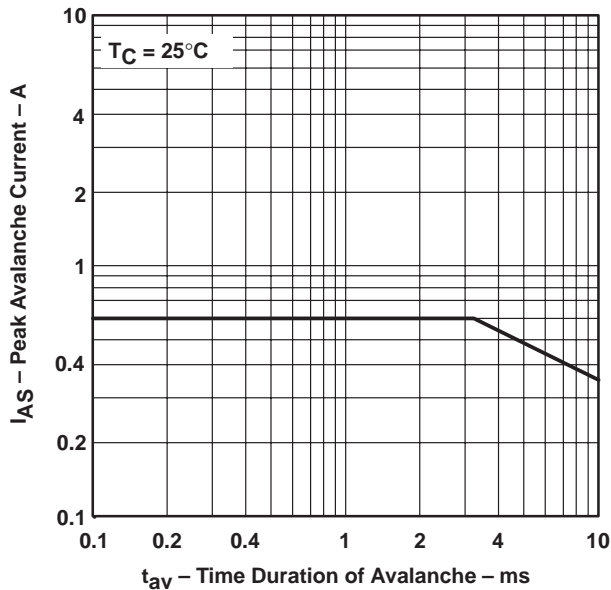


Figure 5

SUPPLY CURRENT  
vs  
FREQUENCY

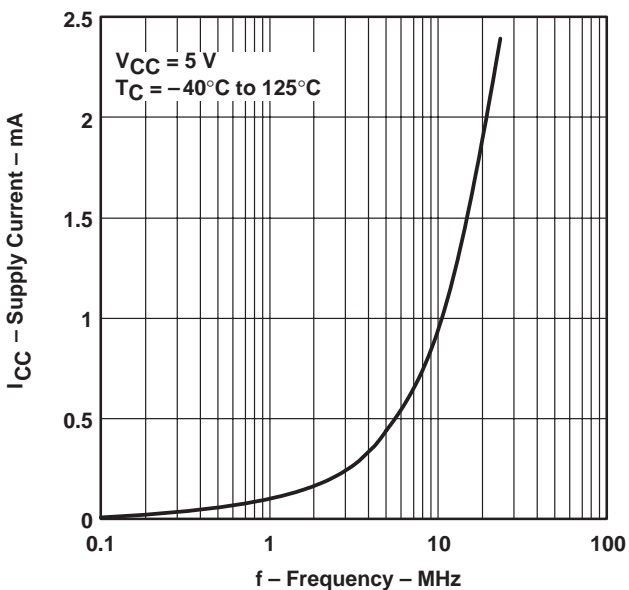


Figure 6

DRAIN-TO-SOURCE ON-STATE RESISTANCE  
vs  
DRAIN CURRENT

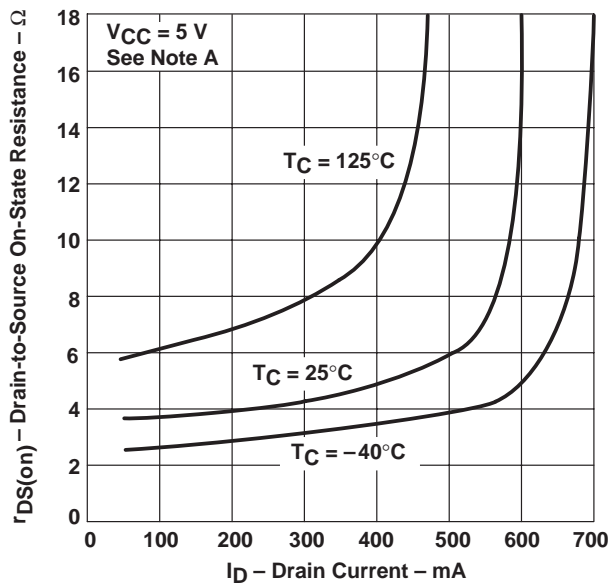


Figure 7

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE  
vs  
LOGIC SUPPLY VOLTAGE

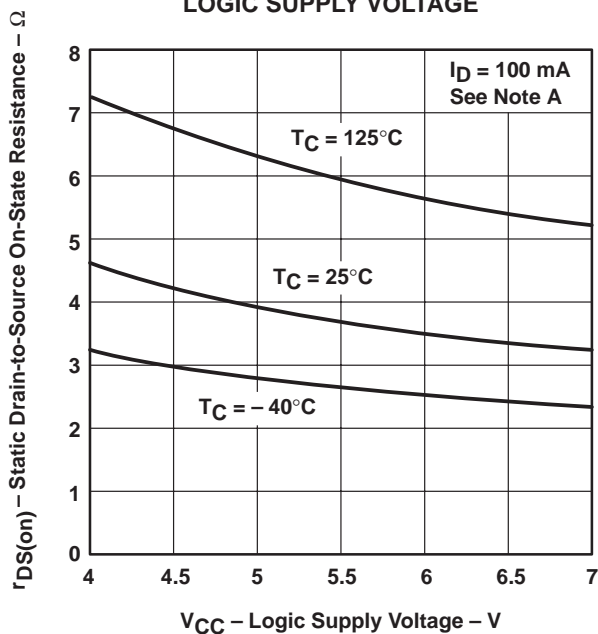


Figure 8





TYPICAL CHARACTERISTICS

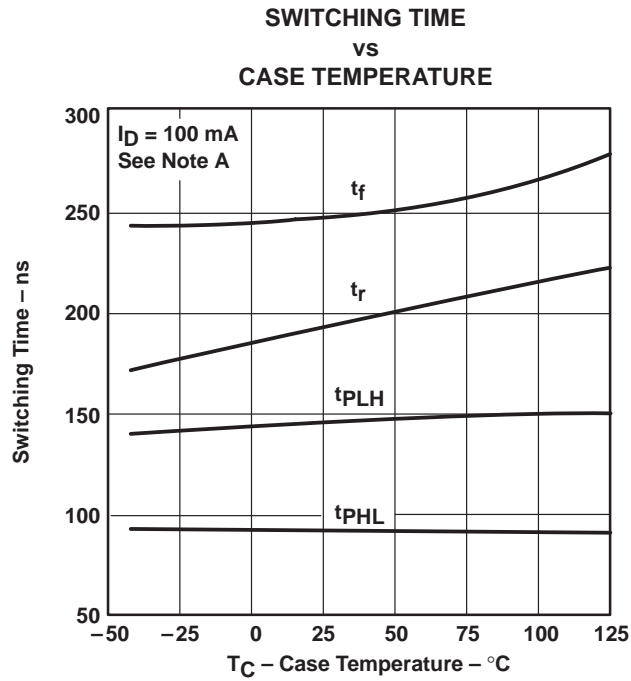


Figure 9

NOTE A: Technique should limit  $T_J - T_C$  to 10°C maximum.

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## THERMAL INFORMATION

**MAXIMUM CONTINUOUS  
DRAIN CURRENT OF EACH OUTPUT  
vs  
NUMBER OF OUTPUTS CONDUCTING  
SIMULTANEOUSLY**

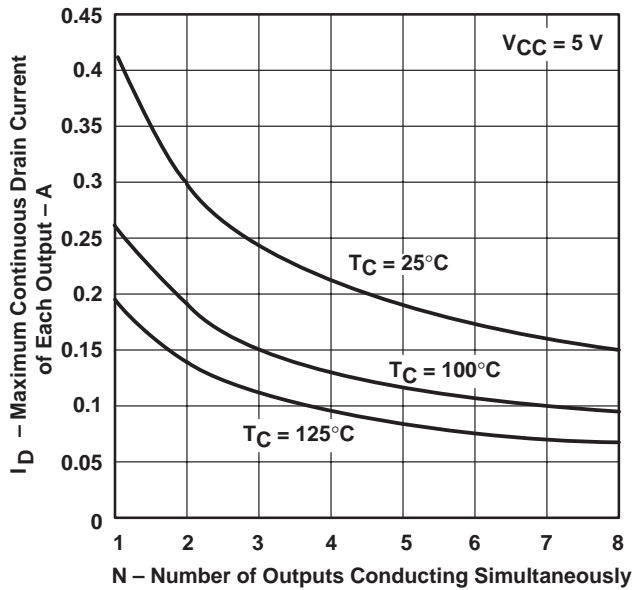


Figure 10

**MAXIMUM PEAK DRAIN CURRENT  
OF EACH OUTPUT  
vs  
NUMBER OF OUTPUTS CONDUCTING  
SIMULTANEOUSLY**

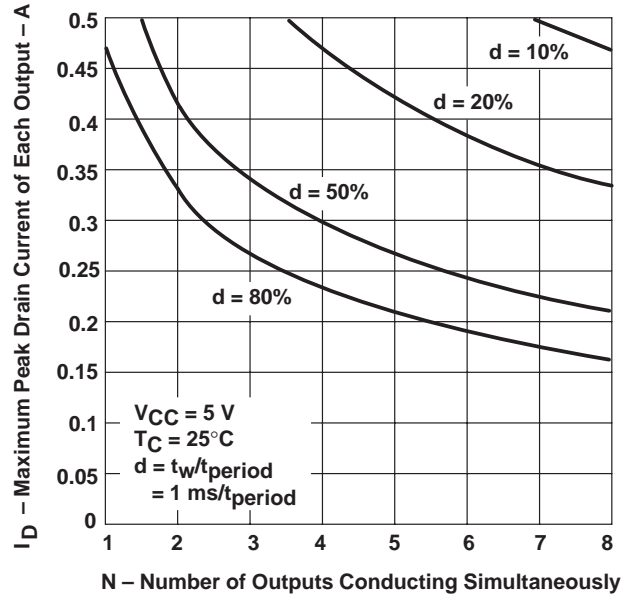


Figure 11

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